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| EXAMINER | |
|---|---|
| SPITTLE, MATTHEW D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2111 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/814,074 | WALKER ET AL. | |
| | Examiner | Art Unit | |
| | Matthew D. Spittle | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1 – 20 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 4, 6 – 12, and 15 – 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yoo et al.

Regarding claim 1, Yoo et al. describe a memory device, comprising:

An address bus interface (column 4, lines 27 – 29; Figure 4, items 410a, 410b);

An address bus termination circuit that can be enabled or disabled (Figure 4, items enclosed by boxes 420, 440; column 5, line 57 – column 6, line 13);

An address bus termination control signal input (Figure 2; where the input is interpreted as the input to the switches SW3, SW4, SW5, SW6 connected to items CON1, CON2) wherein the address bus terminal control signal input is operable to enable the address bus termination circuit when the address bus termination control

signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 2, Yoo et al. describe the address bus termination circuit to be enabled if an asserted address bus termination control signal (Figure 2, items CON1, CON2) is received at the address bus termination control signal input (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 3, Yoo et al. describe the address bus termination circuit to be disabled if the address bus termination circuit control signal (Figure 2, items CON1, CON2) is not asserted (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 4, Yoo et al. describe wherein the address bus termination control signal (Figure 2, items CON1, CON2) is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 6, Yoo et al. describe a data bus interface (column 4, lines 27 – 29; Figure 4, items 410a, 410b) and a data bus termination circuit (column 4, lines 27 – 33; column 5, lines 11 – 13).

Regarding claim 7, Yoo et al. describe a data bus termination control signal input, the data bus termination circuit to be enabled in response to an asserted data bus termination control signal (Figure 4, items enclosed by boxes 420, 440; column 5, line 57 – column 6, line 13; Examiner notes that Yoo et al. describe that their invention can be applied to either address busses or data busses; column 4, lines 27 – 33).

Regarding claim 8, Yoo et al. describe a memory module comprising:

A plurality of memory devices (Figure 4, items 430a, 430b, 450a, 450b) coupled to an address bus in a daisy chain configuration, each of the plurality of memory devices including:

An address bus interface (column 4, lines 27 – 29; Figure 4, items 410a, 410b);

An address bus termination circuit that can be enabled or disabled (Figure 4, items enclosed by boxes 420, 440; column 5, line 57 – column 6, line 13);

An address bus termination control signal input (Figure 2; where the input is interpreted as the input to the switches SW3, SW4, SW5, SW6 connected to items CON1, CON2) wherein the address bus terminal control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 9, Yoo et al. describe wherein for each of the plurality of memory devices the address bus termination circuit to be enabled if an asserted address bus termination control signal (Figure 2, items CON1, CON2) is received at the address bus termination control signal input (column 7, lines 40 – 44 describe where the

control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 10, Yoo et al. describe wherein for each of the plurality of memory devices the address bus termination circuit to be disabled if the address bus termination circuit control signal (Figure 2, items CON1, CON2) is not asserted (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 11, Yoo et al. describe wherein for each of the plurality of memory devices the address bus termination control signal (Figure 2, items CON1, CON2) is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 12, Yoo et al. describe wherein all but the last memory device in the daisy chain configuration has its address bus termination control signal input tied to

ground and the last memory device in the daisy chain configuration has its address bus termination control signal tied to a positive voltage (Figure 7 shows a number of scenarios. In the case where Figure 2, item 420 is module 1, and Figure 2, item 440 is module 2 (here, interpreted as the last memory device in the daisy chain configuration), Figure 7 shows in the table where Module 1 active termination is OFF and Module 2 active termination is ON. In that case, as described in column 7, lines 40 – 44, when a termination resistor is not connected, the CON signal is low (i.e., ground). When, as described in column 8, lines 5 – 10, the termination resistor is connected, the CON signal is high (i.e., a positive voltage). Therefore, Yoo et al. implicitly describes this limitation.

Regarding claim 15, Yoo et al. describe a data bus interface (column 4, lines 27 – 29; Figure 4, items 410a, 410b) and a data bus termination circuit (column 4, lines 27 – 33; column 5, lines 11 – 13).

Regarding claim 16, Yoo et al. describe a data bus termination control signal input, the data bus termination circuit to be enabled in response to an asserted data bus termination control signal (Figure 4, items enclosed by boxes 420, 440; column 5, line 57 – column 6, line 13; Examiner notes that Yoo et al. describe that their invention can be applied to either address busses or data busses; column 4, lines 27 – 33).

Regarding claim 17, Yoo et al. describe a method, comprising:

Connecting in a daisy chain configuration an address bus to (Figure 4, items 410a, 410b; column 4, lines 27 – 29) a plurality of memory devices (Figure 4, items 430a, 430b, 450a, 450b) on a memory module (Figure 4, items 420, 440);

Providing address bus termination circuitry in the plurality of memory devices (Figure 4, items enclosed by boxes 420, 440; column 5, line 57 – column 6, line 13);

Enabling the address bus termination circuitry of only one of the plurality of memory devices (Figure 7 shows a table where only one particular "rank" (interpreted as a memory device) of a memory module has its termination circuitry enabled (turned on).

Regarding claim 18, Yoo et al. describe wherein enabling the address bus termination circuitry of only one of the plurality of memory devices includes enabling the address bus termination circuitry of the last memory device in the daisy chain configuration (Figure 7 shows a number of scenarios. In the case where Figure 2, item 420 is module 1, and Figure 2, item 440 is module 2 (here, interpreted as the last memory device in the daisy chain configuration), Figure 7 shows in the table where Module 1 active termination is OFF and Module 2 active termination is ON. In that case, as described in column 7, lines 40 – 44, when a termination resistor is not connected, the CON signal is low (i.e., disabled). When, as described in column 8, lines 5 – 10, the termination resistor is connected, the CON signal is high (i.e., enabled). Therefore, Yoo et al. implicitly describes this limitation).

Regarding claim 19, Yoo et al. describe wherein enabling the last memory device in the daisy chain configuration includes coupling an address bus termination control pin to a positive voltage (Figure 7 shows a number of scenarios. In the case where Figure 2, item 420 is module 1, and Figure 2, item 440 is module 2 (here, interpreted as the last memory device in the daisy chain configuration), Figure 7 shows in the table where Module 1 active termination is OFF and Module 2 active termination is ON. In that case, as described in column 7, lines 40 – 44, when a termination resistor is not connected, the CON signal is low (i.e., ground). When, as described in column 8, lines 5 – 10, the termination resistor is connected, the CON signal is high (i.e., a positive voltage). Therefore, Yoo et al. implicitly describes this limitation).

Regarding claim 20, Yoo et al. describe wherein enabling the address bus termination circuitry of only one of the plurality of memory devices includes disabling the address bus termination circuits in all but the last memory device in the daisy chain configuration by coupling address bus termination control pins on all but the last memory device to ground (Figure 7 shows a number of scenarios. In the case where Figure 2, item 420 is module 1, and Figure 2, item 440 is module 2 (here, interpreted as the last memory device in the daisy chain configuration), Figure 7 shows in the table where Module 1 active termination is OFF and Module 2 active termination is ON. In that case, as described in column 7, lines 40 – 44, when a termination resistor is not connected, the CON signal is low (i.e., ground). When, as described in column 8, lines

5 – 10, the termination resistor is connected, the CON signal is high (i.e., a positive voltage). Therefore, Yoo et al. implicitly describes this limitation).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. in view of Janzen et al.

Regarding claim 5, Yoo et al. fail to teach wherein the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

Janzen et al. teach that it is well known in the art to reverse logic states (column 2, lines 25 – 33) since one permutation may permit a simpler, yet functionally equivalent design.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the memory device of Yoo et al. to reverse logic states as taught by Janzen et al., and designate the control signal as being asserted when at a logically low level instead of a logic high level. This would have been obvious in order to permit a simpler, yet functionally equivalent design.

* * *

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. in view of Janzen et al.

Regarding claim 13, Yoo et al. fail to teach wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

Janzen et al. teach that it is well known in the art to reverse logic states (column 2, lines 25 – 33) since one permutation may permit a simpler, yet functionally equivalent design.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the memory device of Yoo et al. to reverse logic states as taught by Janzen et al., and designate the control signal as being asserted

when at a logically low level instead of a logic high level. This would have been obvious in order to permit a simpler, yet functionally equivalent design.

Regarding claim 14, Yoo et al. teach the additional limitation wherein all but the last memory device in the daisy chain configuration has its address bus termination control signal input tied to ground and the last memory device in the daisy chain configuration has its address bus termination control signal tied to a positive voltage (Figure 7 shows a number of scenarios. In the case where Figure 2, item 420 is module 1, and Figure 2, item 440 is module 2 (here, interpreted as the last memory device in the daisy chain configuration), Figure 7 shows in the table where Module 1 active termination is ON and Module 2 active termination is OFF. In that case, as described in column 7, lines 40 – 44, when a termination resistor is not connected, the CON signal is low (i.e., ground). When, as described in column 8, lines 5 – 10, the termination resistor is connected, the CON signal is high (i.e., a positive voltage). Therefore, Yoo et al. implicitly describes this limitation.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cottingham can be reached on 571-272-7079. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

JOHN R. COTTINGHAM
PRIMARY EXAMINER